Centipede Playfield RAM Testing the Playfield RAM

1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as follows:
   a. Press TESTER RESET
   b. DBUS SOURCE TO ADDR
   c. BYTES to 1024
   d. R/W MODE to (OFF)
   e. R/W to WRITE
   f. Key in 0400
   g. Set R/W MODE to PULSE, then to OFF.
   h. R/W to READ
   i. Set R/W MODE to PULSE, then to OFF.
3. If the CAT Box reads an address that doesn't compare, the COMPARE ERROR LED lights, the ADDRESS/SIGNATURE display shows the failing address location, and the ERROR DATA DISPLAY switch is enabled.
4. If the COMPARE ERROR LED does not light, rekey 0400 and repeat the test with the DBUS SOURCE switch set to ADDR. This ensures that the data bits at address 0400 will go high. If the COMPARE ERROR LED does not light after this step, the Playfield RAM is good.

Playfield Address Selector

The Playfield Address Selector controls the access to the playfield memory. It allows either the game MPU or the sync generator to scan the playfield memory. The Playfield Address Selector consists of multiplexers P5, and P7 and gate K4.

When $\overline{4H}$ on pin 1 of P5 and P7 is low and pin 15 on P7 is low, the Playfield Address Selector receives 8H, 16H, 32H, and 64H on P5 and 16V, 32V, 64V, and 128V on P7 from the sync generator. These signals enable the sync generator circuits to access the playfield memory.

When $\overline{4H}$ goes high the game MPU addresses the playfield memory (via AB0-AB9) for the positioning of the graphics. During horizontal blanking (pin 15 of P7 is high) the outputs of P7 (PFA4-PFA7) are held high enabling the motion object circuitry to access the playfield memory for the motion objects to be displayed.

Playfield Multiplexer

The Playfield Multiplexer receives playfield data from the playfield memory (PFD0-PFD31) and the output (PF0-PF7) is a code that determines what is 1) displayed on the monitor, or 2) read or updated by the MPU. The Playfield Multiplexer consists of select multiplexers K6, L6, M6, N6 and P6.

When 256H is low and 4H is high, AB4 and AB5 from the MPU address bus is the selected output from P6. This output is applied to multiplexers K6, L6, M6, and N6 as select inputs. When the MPU is accessing the playfield code multiplexer, the playfield data is either being read or updated by the MPU. When 256H is high and 4H is low, the inputs from the sync generator (128H and 8V) are the selected outputs. These signals then select which bits of data PFD0-PFD31 are sent out via K6, L6, M6, and N6 for the playfield codes that eventually are displayed on the monitor.

The playfield codes (PF0-PF7) are latched by J5 and J6 to the MPU data bus (J5) and to the picture data PROM circuitry (J6). When $\overline{PFRAM}$ is low and 1H from the sync generator goes high, the inputs on J5 (PF0-PF7) are latched out to the MPU via DB0-DB7. When 4H on pin 11 of J6 goes high, the inputs (PF0-PF7) are latched to the picture data PROM circuitry.

Picture Data ROM Circuitry

The picture data ROM circuitry receives picture information, assigns a color code to the information and sends it to the color PROM circuitry. The picture data ROM circuitry consists of ROM devices F7 and H/J7, multiplexers F8, H8, J8, K8, shift registers H9 and J9, and latch F9.

The picture ROMs receive (PIC0-PIC5) from the playfield code multiplexer, MGA0-MGA3 (motion graphics address) from the motion object circuitry, 256H and $\overline{256H}$ from the sync generator. PIC0-PIC5 represent the code for the object to be displayed. MGA0-MGA3 set one of eight different combinations of the 8-line by 8-bit blocks of picture video or the 16 line by 8 bit blocks of motion object video.

256H when high selects the playfield picture color codes to be addressed. 256H when low selects the motion object color codes to be addressed. The picture data ROM output D1-D8 on F7 and H/J7 are multiplexed by F8, H8, J8 and K8 and shifted out serially at H9 and J9. This serial output is latched by F9 as AREA0 and AREA1 to the motion object horizontal circuitry and the video output circuit.

Motion Object Circuitry (Vertical)

The Motion Object Circuitry (vertical) receives playfield data and vertical inputs from the sync generator circuitry to generate the vertical component of the motion object video. PFD8-15 from the playfield memory and 1V-128V from the sync generator are compared at F6 and H6. The output is gated by A7 when a motion object is on one of the sixteen vertical lines and is latched by E6 to AND gate B7. A low on B7 pin 8 indicates the presence of a motion object on one of the vertical lines during non-active video time. This signal (MATCH) enables the multiplexers in the picture data circuitry.

When 256H on pin 1 of D7 goes high, 1V, 2V, 4V and PIC0 are selected. When 256H goes low, the latched output of E6 is selected. The output of D7 is EXCLUSIVE OR gated at E7 and is sent to the picture data selector circuitry as motion graphic address (MGA0-MGA3). The other input to EXCLUSIVE OR gate E7 is PIC7 from the playfield code multiplexer circuitry. PIC7 when high causes the output of E7 to be complimented. For example, if MGA0-MGA3 are low, PIC7 causes MGA0-MGA3 to go high. This causes the motion object video to be inverted top to bottom.

Motion Object Circuitry (Horizontal)

The motion object circuitry (horizontal) receives playfield data and horizontal inputs from the sync generator circuitry. PFD16-PFD23 from the playfield memory determine the horizontal position of the motion object. PFD24-PFD29 from the playfield memory determine the indirect color of the motion object. PFD16-PFD23 are latched by L7 and loaded into the horizontal position counters A5 and B5 by a low on pin 9. The horizontal position counters then address video RAMs A6 and B6. These RAMs are loaded with the video data for the particular motion object from shift registers H9 and J9 (which were loaded from the graphics ROM). The output for RAMs A6 and B6 is then sent to the color PROM circuitry as MR0 and MR1.

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